

## Low Power – Low Leakage SRAM

**TECHNOLOGY: 180nm SMIC G**  
**Status: silicon OK**

### KEY FEATURES

- large supply voltage range: 1 – 2V
- low leakage design (worst case, high temperature 100pA/byte)
- storage capacity: 256B / 2kB ready (or custom size on demand)
- low power stand-by state (data retain, no access)
- CLEARN command for optional memory bank initialization

### SHORT DESCRIPTION

The synchronous RAM is a fully static memory with write enable (WEN), chip enable (CEN), address (A), data in (D) and data out (Q) pins. The RAM is self-timed and is designed for very low leakage application in a standard CMOS process with 3.3V option (no need for low-leakage, i.e. LL, technology option). All synchronous inputs are latched on the rising-edge of the clock signal. When CEN is low and WEN is high the RAM is in read mode. If both CEN and WEN are low the input data D is stored in the memory and it is forwarded to Q (write-through mode).

If CEN is high the memory is deselected and forced into a low-power standby mode. Stored data is fully retained but memory access is disabled for data read or data write, the existing data outputs continue to drive their previous values.

When OEN is active (low) the data out Q is valid. When OEN is high the output data Q is high-Z.

PD active high, drives the memory in power-down mode: data are lost, no read/write is accessible and the RAM has virtually zero leakage consumption.

CLEARN (active low) writes all 0 data in the memory and it is sometimes used as RAM initialization command in specific application.

### Deliverables files:

GDS, CLD, lib, verilog

### APPLICATIONS

Mixed-signal IC, ASIC, digital IC, low leakage analog and digital design, battery assisted RFID.

### PIN FUNCTIONS

#	NAME	DESCRIPTION	NOTE
1	VSS	Ground	
2	VDD	Supply	
3	A<0:10>	Address bus (note1) (A[0]=LSB)	
4	WEN	Write Enable (active low)	
5	OEN	Output Enable (active low)	
6	CLEARN	Clear (active low)	
7	CEN	Chip enable (active low)	
8	PD	Power Down	
9	CK	Clock signal	
10	D<0:7>	Data Input (D[0]=LSB)	
11	Q<0:7>	Data Output (Q[0]=LSB)	

Note 1: The address bus size, depends on the memory size. For 2kB SRAM, 11 address bits are used.

### OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
VDD	Supply voltage	1	2	V
T	Storage temperature	-40	85	°C

## 2kB SRAM CHARACTERISTICS

### PHYSICAL DIMENSIONS

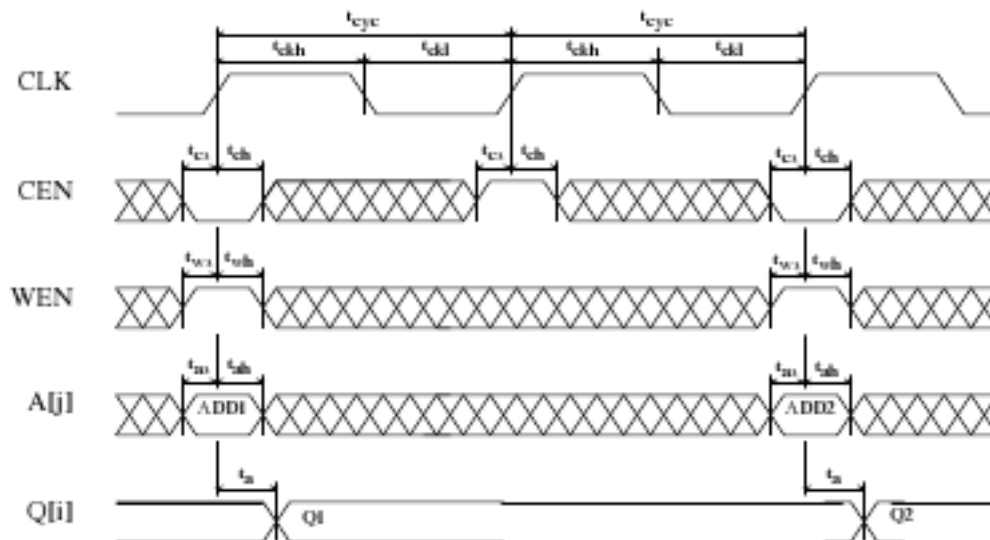
Area type	Width( $\mu\text{m}$ )	Height( $\mu\text{m}$ )	Area( $\mu\text{m}^2$ )
Footprint	720	420	302400

### ELECTRICAL CHARACTERISTICS

Conditions: VDD from 1 to 2V, T 27°C, CEN=0, unless otherwise stated.

Parameter	Condition	Min	Typ	Max	Unit	Note
Current Consumption	IDD	Power Down mode		2.55	nA	
		Stand by mode		210	nA	
		Read/Write mode		75	$\mu\text{A}$	
Clock frequency	fck		10		MHz	
High-level output voltage	VOH		VDD			
Low-level output voltage	VOL		0			
Rise and fall time	tr/ff	Evaluated at 20% - 80% levels	2		ns	

### Read cycle timing



### Write cycle timing

