

SS0206 30 BIT Video LVDS Receiver

TECHNOLOGY: SMIC 90nm G

Status: waiting for silicon

KEY FEATURES

- up to 5.95Gbps ($f_{ck}=170\text{MHz}$) data rates (DDR)
- Single 3.3V supply for I/O
- Single 1.0V supply for core
- CMOS/TTL level Output
- Low power consumption (80mA typical)
- Power Off Protection
- Operating Temperature Range: -40 to +125°C

APPLICATIONS

Video SerDes Link: FPD-Link II

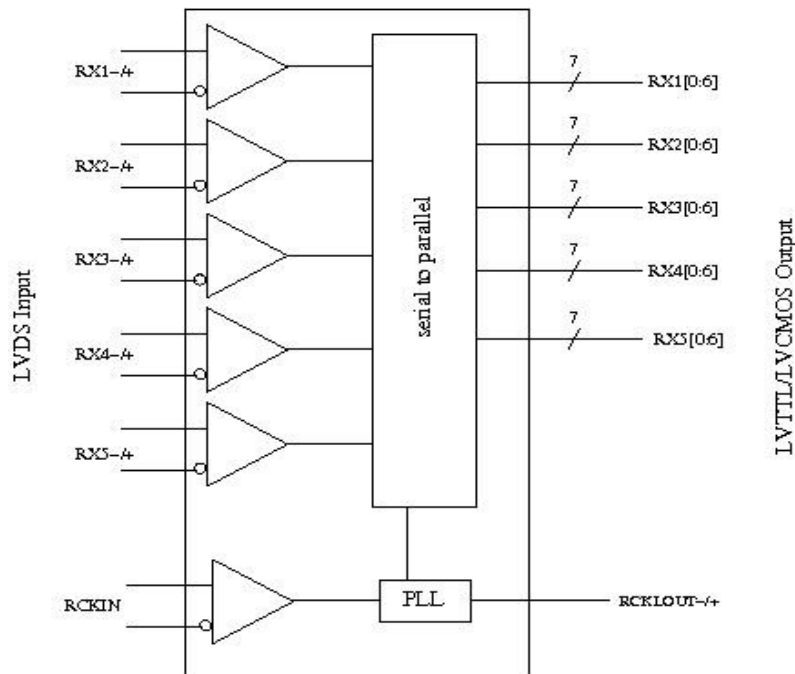
SHORT DESCRIPTION

The SS0206 is a LVDS Deserializer designed to support data transmission between a Host and a Flat Panel Display (FPD) from NTSC up to SXGA+ resolution. The device converts five LVDS data stream back to 35 bits of CMOS/TTL parallel data: 30 bit of RGB data and 5 timing and control bits (H/VSYNC, DE, CTRL1/2).

At the maximum transmit clock frequency of 170MHz, the maximum transmission rate of each LVDS line is up to 1.19Gbps, corresponding to a data throughput of 5.95Gbps.

The SerDes exhibits a low current consumption if compared to similar products available on the market.

BLOCK DIAGRAM



OPERATING CONDITIONS

Parameter	Condition	Min	Typ	Max	Units
VDD10	Supply voltage for core circuit	0.9	1.0	1.1	V
VDD33	Supply voltage for I/O circuit	3.0	3.3	3.6	V
T _A	Operating junction temperature	-40		+125	°C

DC ELECTRICAL CHARACTERISTICS

 (VDD10 = +0.9 to +1.1V, VDD33 = +3.0 to +3.6V, T_A = -40 to +125°C, R_L = 100Ω)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Differential Input High threshold	V _{TH}				100	mV
Differential Input low threshold	V _{TL}		-100			mV
Input Common Mode	V _{ICM}		0.1	1.25	2.00	V

CURRENT CONSUMPTION

 (VDD10 = +0.9 to +1.1V, VDD33 = +3.0 to +3.6V, T_A = -40 to +125°C, R_L = 100Ω)

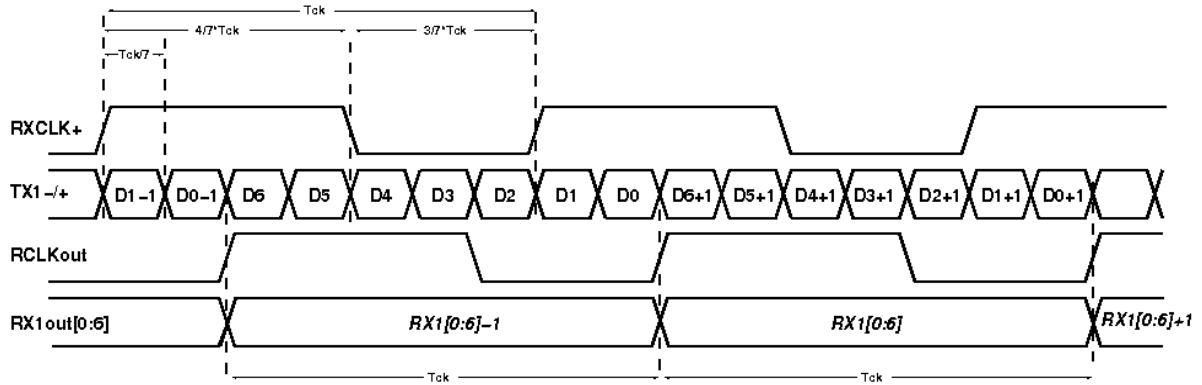
Parameter	Symbol	Condition	Min	Typ	Max	Units
3.3V Supply Current	I _{CC33}	f _{CK} =170MHz		20		mA
1.0V Supply Current	I _{CC10}	f _{CK} =170MHz		60		mA

SWITCHING ELECTRICAL CHARACTERISTICS

 (VDD10 = +0.9 to +1.1V, VDD33 = +3.0 to +3.6V, V_{CM} = 1.25V, T_A = -40 to +125°C, R_L = 100Ω)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Clock Freq. (RCKLOUT)	f _{ck}		5		170	MHz

AC TIMING DIAGRAM



Data output: the single LVDS data stream with data rate up to 1.19Gbps, is converted back to seven parallel data with RCLKOUT of 170MHz.

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