

SS0106 30-BIT Video LVDS Transmitter

TECH : SMIC 90nm G
Status: waiting for silicon

KEY FEATURES

- up to 5.95Gbps ($f_{CK}=170\text{MHz}$) data rates (DDR)
- programmable Pre-emphasis
- Single 3.3V supply for I/O
- Single 1.0V supply for core
- LVDS Output
- Low power consumption (60mA typical)
- Power Off Protection (outputs in TRI-STATE)
- Operating Temperature Range: -40 to +125°C

APPLICATIONS

Video SerDes Link: FPD-Link II

SHORT DESCRIPTION

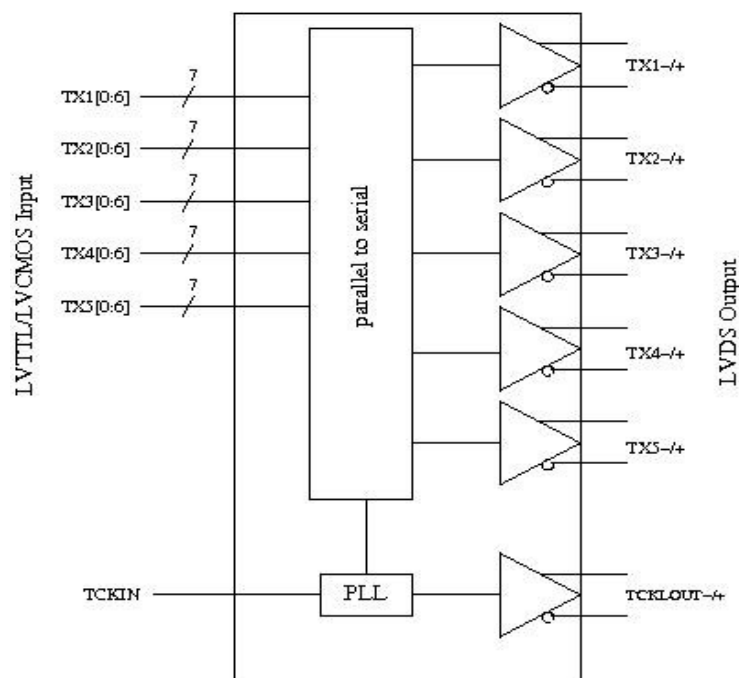
The SS0106 is a LVDS Serializer designed to support data transmission between a Host and a Flat Panel Display (FPD) from NTSC up to SXGA+ resolution. The SS0106 converts 35bits of CMOS/TTL data into LVDS data stream (over 5 impedance controlled 100Ohm lines).

At the maximum transmit clock frequency of 170MHz, 30-bits of RGB data and 5 timing and control bits (H/VSYNC, DE, CTRL1/2) are transmitted with a data throughput as high as 5.95Gb/s, corresponding to 1.19Gb/s per LVDS channel.

By LVDS TX pad with programmable pre-emphasis, the SerDes is able to drive UTP cable as long as 10m cat the maximum data throughput. The LVDS pad can be set in high-impedance state through Enable Input (EN), dropping the device to an ultra-low-power state.

The SerDes exhibits a low current consumption if compared to similar products available on the market.

BLOCK DIAGRAM



OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Units
VDD10	Supply Voltage for core circuit	0.9	1.0	1.2	V
VDD33	Supply Voltage for I/O circuit	3.0	3.3	3.6	V
T _A	Operating junction temperature	- 40		+125	°C

PRE-EMPHASIS LEVELS

Data rate-per-channel	Input clock frequency	Data throughput	PE level	Max cable length [m]
1190 Mbps	170MHz	5.950Gbps	extra	30
1190 Mbps	170MHz	5.950Gbps	strong	20
1190 Mbps	170MHz	5.950Gbps	medium	15

DC ELECTRICAL CHARACTERISTICS

 (VDD10 = +0.9 to +1.3V, VDD33 = +3.0 to +3.6V, T_A = -40 to +125°C, R_L = 100Ω, EN = VDD)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Differential Output Voltage	V _{OD}	R _L = 100Ω	250	350	450	mV
V _{OD} Magnitude Change	ΔV _{OD}				35	mV
Offset Voltage	V _{OS}	R _L = 100Ω	1.125	1.25	1.375	V
Offset Magnitude Change	ΔV _{OS}				25	mV
Differential output Short-Circuit Current	I _{OSD}	EN=VDD, V _{OD} = 0		3.5	4.2	mA
Output High-Impedance Current	I _{OZ}	EN= Low, OUT+ = 0 or VDD OUT- = 0 or VDD R _L = ∞	-10		10	μA
Power-Off Output Current	I _{OFF}	VDD = 0 or open, OUT+ = 0 or 3.6V, OUT- = 0 or 3.6V, R _L = ∞	-15		15	μA

CURRENT CONSUMPTION

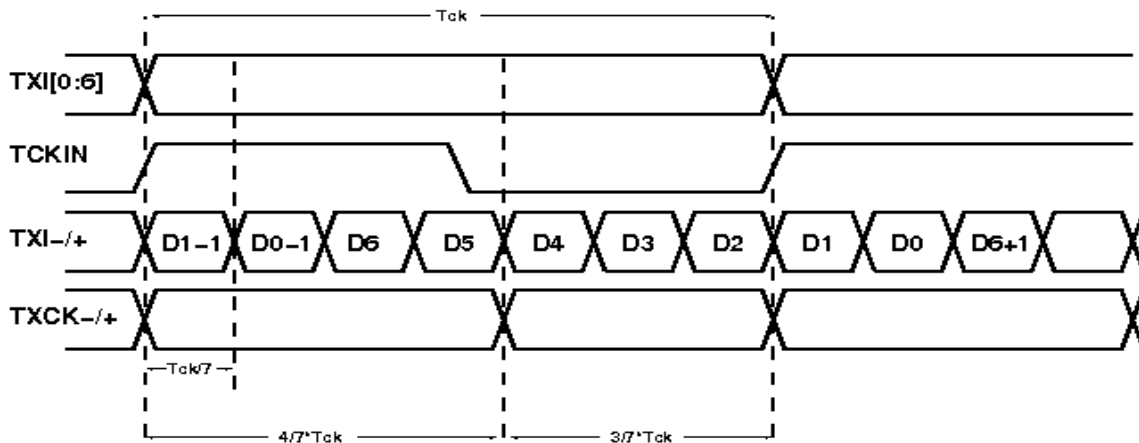
 (VDD10 = +0.9 to +1.1V, VDD33 = +3.0 to +3.6V, T_A = -40 to +125°C, R_L = 100Ω)

Parameter	Symbol	Condition	Min	Typ	Max	Units
3.3V Supply Current	I _{CC33}	EN=VDD, f _{CK} =170MHz		19		mA
1.0V Supply Current	I _{CC10}	EN=VDD, f _{CK} =170MHz		41		mA

SWITCHING ELECTRICAL CHARACTERISTICS

 (VDD10 = +0.9 to +1.1V, VDD33 = +3.0 to +3.6V, V_{CM} = 1.25V, TA = -40 to +125°C, RL = 100Ω, EN = VDD)

Parameter	Symbol	Min	Typ	Max	Units
Clock Freq. (TCKIN)	f _{ck}	5		170	MHz
Rise Time (10%→90%)	t _{TLH}		0.65	1	ns
Fall Time (90%→10%)	t _{THL}		0.65	1	ns
Disable Time High to Z	t _{PHZ}		1.82	2.2	ns
Disable Time Low to Z	t _{PLZ}		1.90	2.3	ns
Enable Time Z to High	t _{PZH}		2.3	2.8	ns
Enable Time Z to High	t _{PZL}		1.94	2.4	ns

AC TIMING DIAGRAM


LVDS Output: at a transmitter clock frequency TCKIN, 7 bits of LVCMOS/LVTTL data (TX1[0:6]) are transmitted into the LVDS channel at an effective rate seven times the clock frequency.

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