JUNIOR DESIGNER
Curriculum Vitae

Educational

Title	Date (since–to)	Institute	Activities
Ph.D. in Information Technology	2013-2015	University of Parma. Sponsored by STM.	Thesis title: Design Strategies and Modelling of Low-Power Sigma-Delta Analog-to-Digital Converters. Activity: design, layout and lab. testing of Sigma-Delta ADCs in 90-nm STM technology.
Master Degree Thesis	October 2011 - March 2012	University of Parma. Sponsored by STM.	Thesis title: Design of a Switched Capacitor DC-DC converter for portable devices. Activity: analysis and high-level simulations of the DC-DC converter with Matlab Simulink. Transistor-level design of the converter and its control in 65-nm STM technology.
Masters degree in Electronic Engineering	2009-2012	University of Parma	Design of Analog and Digital ICs. Design of Electric Drives for Industrial Automation. Semiconductor devices.
Bachelor degree in Electronic Engineering	2006-2009	University of Parma	Basics of analog and digital electronics, power electronics and data communications.
High School Graduate	2001-2006	Technical Industrial Institute A. Berenini	Programming Languages: C, C++.

Foreign Language

Language	Knowledge
English	Good knowledge of spoken and written English
French	Basic knowledge of spoken French

Work Experience

Company	Date (since–to)	Job title	Main Activities
Consultant at Silis s.r.l., Parma (Italy) – IC Design and consulting company	2012 - 2015	Analog/Mixed-Signal IC designer	Design, layout and lab testing of: 16 bit Sigma-Delta A/D converters in STM 65/90nm. Ultra Low power and Low Noise op-amp design. Low Power Relaxation Oscillator for Sensor-RFID.
	October 2014 - November 2014	Design service at Maxim Integrated (Milano, Italy)	Design and layout of Sigma-Delta low-noise op-amp in MAXIM 180nm.
	January 2015 – March 2015	Analog/Mixed-Signal IC layout	Layout of low power bandgap, relaxation oscillator, opamps and 14 bit Sigma Delta A/D converter in AMS 350nm
Employee at Silis s.r.l., Parma (Italy) – IC Design and consulting company	January 2016 – May 2016	Design service at AMS AG (Pisa, Italy)	Activity: Design verification and characterization of an 8-bit ADC Pipeline. Design of buffer reference op-amps in AMS 180nm.
	June 2016 – September 2016	Design service at AMS AG (Pavia, Italy)	Activity: Design and verification of class-AB op-amp, LNA and S/H. Top level verification in AMS 350nm.
	October 2016 – September 2017	Analog/Layout Designer at Silis s.r.l. (Parma, Italy)	Activity: Design and Layout of some blocks of a 12b, 128MS/s pipeline ADC.
	October 2017 – Now	Design service at STM (Milano, Italy)	Activity: Design of Regulators, bandgap (with second order compensation), oscillator, INA. Top level simulation. Technology: BCD

IT/CAD knowledge

Category	Applications
Design and Simulation Systems	Systems CadenceTM Virtuoso Composer and ADE flow up to 6.0, ADE, SpectreTM, SpectreRFTM, OCEANTM; Mentor GraphicsTM Design Architect IC, EldoTM.
Analog IC layout	CadenceTM Virtuoso Layout/Layout XL flow, Assura, Mentor GraphicsTM Calibre.
Mixed Signal IC	CadenceTM ICMS/ICFB, AMS-Designer plug-in.

Digital IC design	basic VHDL language.
PCB design	CadenceTM Pspice,Orcad Capture and Layout.

Job skills

Category	Applications
Analog/Mixed signal IC design	Good knowledge of design methodology for low power/voltage analog cells.
Analog/Mixed signal IC layout	Good analog layout experience with parasitic and area optimization.
Lab testing	Good knowledge of standard lab. instrumentation and experience in samples testing and characterization.
Relational skills and flexibility	Availability to travel abroad (short periods), good relational skills, able to work in dynamic environment with flexible timetable.

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