LAYOUT ENGINEER
Curriculum Vitae

Educational

Title	Date (since–to)	Institute	Activities
High School Graduate	2004-2009	Scientific High School Galileo Galilei, PA, ITA	Graduation marks: 90/100
Bachelor degree in Electronic Engineering	2009-20016	University of Palermo, ITA	Basics of analog and digital electronics and data communications. **Graduation marks: 95/110**
Masters degree in Electronic Engineering	2009-2016	University of Modena, ITA	Design of Analog and Digital ICs. Layout of Analog ICs Semiconductor devices. Power electronics. **Graduation marks: 110/110** **Thesis Project:** design and layout of a Li-Fi transmitter in 350nm techn.

Foreign Languages

Language	Knowledge
English	Certification "Trinity-level 10 (C1)"
French	Basic (school) level

Work Experience

Company	Date (since–to)	Job title	Main Activities
Silis s.r.l., Parma, ITA, design and consulting company (www.silis.it)	May 2019 - today	Analog Layout Engineer	Layout of a Baseband LTE receiver (NB-IoT) in 28nm SOI: -Operational Amplifier, -Variable gain amplifier -$\Sigma\Delta$ A/D converter -Centralized Bias -High frequency decimator (digital) -Test mode control block (digital) -Padring

IT/CAD knowledge

Category	Applications
Design and Simulation Systems	Systems CadenceTM Virtuoso Composer and ADE flow up to 6.0, ADE-L, SpectreTM, Multisim
Analog IC layout	Cadence Virtuoso Layout/Layout XL flow, Assura (DRC/LVS) Mentor Graphics: Calibre (DRC/LVS) Synopsis: StarRC (parasitic extraction)
Digital IC design	VHDL language and programming (basic).
Other Tools	CST, Matlab, LabView
Other Programming Languages	Basic C

Job skills

Category	Applications
Analog IC layout	Analog layout in CMOS technologies (full layout flow with **Cadence/Mentor/Synopsis tools**).
Analog IC design	Design methodology of low power/voltage analog cells.
Lab testing	Basic knowledge of standard lab instrumentation.
Relational skills and flexibility	Availability to travel abroad, good relational skills, able to work in dynamic environment with flexible timetable.

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