SiliS Silicon Solutions

SENIOR DESIGNER
Curriculum Vitae

Educational

Title	Date (since–to)	Institute	Activities
High School Graduate	1993 - 1998	High School of Parma, Technical Industrial Institute "L. da Vinci"	Graduation marks: 60/60
B.Sc. in Electronics Engineering	1998 - 2004	University of Parma (Italy) Faculty of Engineering Course: Electronic Engineering	Graduation marks: 104/110 Thesis title: "Design of CMOS operational amplifier with Rail-to-Rail input and class AB output stage"
M.Sc. in Electronics Engineering	2004 - 2007	University of Parma (Italy) Faculty of Engineering Course: Electronic Engineering	Graduation marks: 110/110 (Summa cum laude) Thesis title: "Design of integrated lock-in amplifier for resonant sensor"
Ph.D.	2008 - 2010	University of Parma (Italy) Department of Information Engineering	Thesis title: "High-Speed Pipeline Analog-to-Digital Converter: Transistor-Level Design and Calibration Issues"

Foreign Language

Language	Knowledge
English	Good knowledge of spoken and written English

Work Experience

Company	Date (since–to)	Job title	Main Activities
University of Parma (Italy) Department of Information Engineering	2007	Scholarship at University of Parma (Italy) Department of Information Eng.	Design of radio-frequency CMOS circuits
University of Parma (Italy) Department of Information Engineering	2010 - 2018	Postdoctoral Research Fellow at University of Parma (Italy) Department of Information Eng.	Design of Analog CMOS circuits: • Example: 12b, 128MS/s pipeline ADC (Design)
Silis s.r.l., Parma (Italy) – design and consulting company	2008 - 2010	Junior Analog IC's designer	Analog circuits design and layout: • DC-DC Buck converter with PFM control (Design and Test) • Operation amplifier for high-speed A/D (Design) • Multiplying D/A stage for pipeline A/D (Design) • Design-oriented modelling of sigma-delta converters (Matlab and Simulink) • Design of Low-noise bandgap reference for 18-bit 1 MHz Sigma-Delta A/D converter • Design of flash analog-to-digital conversion stage for 12-bit 16 MHz Multibit Sigma-Delta A/D converter
	2010-2011	Analog Consultant at Sensor Dynamics (Pisa, Italy)	Analog circuits design and layout: • Design and simulation and layout of operational amplifiers for external n-mos driving • Design and simulation of short circuit comparator for operational amplifier protection • PWM driver design and simulation • Sigma-Delta modulator simulation and verification

	2011-2012	Analog Consultant at Maxim Integrated (Milan, Italy)	• Design and simulation of low-noise and low-power bandgap reference and low-pass filter for noise reduction • Design and simulation of power-on reset circuit • Design and simulation of operational amplifier for voltage references analog buffers • Redesign and optimization of operational amplifiers for voltage reference generation • Redesign and optimization of charge amplifier
	2012-2013	Senior Analog Designer at Silis s.r.l. (Parma, Italy)	• Design, simulation and layout of analog circuits for automotive ASIC interface (R2R D/A converter, Current D/A converter, Voltage and Current references generator, HV protection circuits, etc) • Test and characterization of analog circuits for automotive ASIC interface (Measurement and instrumentation remote control design via Matlab and Labview)
	2014 - 2017	Senior Analog Designer at Silis s.r.l. (Parma, Italy) Test Engineer at Silis s.r.l. (Parma, Italy)	• Design, simulation and layout of analog circuits for automotive ASIC (Back-end and tape-out) • Prototypes test and characterization • ATE design for production volume (Labview application design for analog devices test and verification, pcb design)
	2018	Analog Consultant at AMS (Premstaetten, Austria)	• Analog circuits design for H bridge driving
	2019	Senior Analog Designer at Silis s.r.l. (Parma, Italy)	• Example: 12b, 128MS/s pipeline ADC (IP under validation)

		Test Engineer at Silis s.r.l. (Parma, Italy)	
	2020	Analog Consultant at STMicroelectronics (Milan, Italy)	• Design and simulation of current DAC, voltage and current feedback loops for current/voltage control

IT/CAD knowledge

Category	Applications
Design and Simulation Systems	Systems CadenceTM Virtuoso Composer and ADE flow up to 6.0, ADE, ADE XL, Maestro, SpectreTM, SpectreRFTM, OCEANTM; Mentor GraphicsTM Design Architect IC, EldoTM.
Analog IC layout	CadenceTM Virtuoso Layout/Layout XL flow, Assura, Mentor GraphicsTM Calibre.
Mixed Signal IC	CadenceTM ICMS/ICFB, AMS-Designer plug-in.
Digital IC design	basic VHDL language.
PCB design	CadenceTM Pspice,Orcad Capture and Layout.

Test and Measurement

Category	Applications
Test and measurement	Very good knowledge of test and measurement strategy and equipment.
	Very good knowledge of control programming system in Matlab environment
	Good knowledge of control programming system in Labview environment (i.e. ATE application design)

Job skills

Category	Applications
Analog/Mixed signal IC design	Very good knowledge of design methodology for low power/voltage analog cells.
Analog/Mixed signal IC layout	Very good analog layout experience with parasitic and area optimization.
Lab testing	Good knowledge of standard lab instrumentation and experience in samples testing and characterization.
Relational skills and flexibility	Availability to travel abroad (short periods), good relational skills, able to work in dynamic environment with flexible timetable.

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