# SENIOR DESIGNER
## Curriculum Vitae

## Educational

| Title | Date (since–to) | Institute | Activities |
|---|---|---|---|
| High School Graduate | 1994-1999 | High School of Reggio Emilia, Technical Industrial Institute Leopoldo Nobili | Graduation marks: 100/100 |
| M.Sc. in Electronic Engineering | 1999-2005 | University of Parma (Italy)<br><br>Faculty of Engineering<br><br>Course: Electronic Engineering | Graduation marks: 110/110<br><br>Thesis title: "Design of operational amplifier with bipolar devices input stage for pipeline architecture A/D converter". |
| PHD in Information Technology | 2007-2009 | University of Parma (Italy)<br><br>Information technology Department | Thesis title: "Design and Implementation of successive approximation SAR ADC for mid-high frequency applications". |

## Foreign Language

| Language | Knowledge |
|---|---|
| English | Good knowledge of spoken and written English |
| French | Good knowledge of spoken and written French |

## Work Experience

| Company | Date (since–to) | Job title | Main Activities |
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|---|---|---|---|
| University of Parma (Italy) Department of Information Engineering | 2006 | Intern | Design of SAR architecture A/D converters for low power, high frequency and low resolution applications. |
| Silis s.r.l., Parma (Italy) – design and consulting company | 2008 - 2012 | Senior Analog/Mixed-Signal IC's designer | Design of quartz RTC system. Design of LVDS transceiver system with variable load compensation. Design of SAR architecture A/D converter with high sampling frequency and low power consumption for UWB applications. Design, Layout, Test and Debug of temperature acquisition system whose main characteristics are: Very low current consumption; 0.5°C accuracy in temperature measurement; Temperature Logging; Radio-Frequenza (RF) interface in 860MHz-920MHz range; User manual intarface for logging activation and status check; Calibration interface; Calibration data storing in OTP memory elements; |
| | Oct 2012 – Nov 2012 | Analog Consultant at Maxim Integrated (Milan, Italy) | Layout of: Power Management Unit for MEMS capacitive sensors acquisition chain. |

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| | May 2013 – Oct 2013 | Analog Consultant at Maxim Integrated (Pisa, Italy) | Design and verification of: Power Management Unit for MEMS capacitive sensors acquisition chain; SC filter; RC oscillator; Testability chain; Programmable filter amplifier. |
| | Mar 2014 – Aug 2014 | Analog Consultant at Maxim Integrated (Pisa, Italy) | Design and Layout of: Power Management Unit for MEMS capacitive sensors acquisition chain. |
| | Sep 2014 – May 2015 | Analog Consultant at ams AG (Unterpremstaetten, Austria) | Design of: Design of high-voltage bridge-driver for PWM motor control supporting current sensing; Design of high-voltage charge-pump; |
| | Jul 2015 – Nov 2015 | Analog Consultant at ams AG (Unterpremstaetten, Austria) | Design of: Programmable Relaxation Oscillator; Smart controllable Pull-Down Resistance for very low voltage supply. |
| | Dic 2015 – Aug 2016 | Analog Consultant at ams AG (Valencia, Spain) | Design of: Power Management Unit for MEMS capacitive sensors acquisition chain and Temperature acquisition chain. |
| | Sep 2016 – Sep 2017 | Analog Consultant at ams AG (Rapperswil, Switzerland) | Design of: OSC, LDO, Charge-Pump for, top level simulations for MEMS capacitive sensors. |
| | Oct 2017 – Now | STMicroelectronics (Milan, Italy) | Design of a READER stage for Preamp used in Magneto Recording Hard Disk |

## IT/CAD knowledge

| Category | Applications |
|---|---|
| Design and Simulation Systems | Systems Cadence™ Virtuoso Composer and ADE flow up to 6.0, ADE, Spectre™, SpectreRF™, OCEAN™; Mentor Graphics™ Design Architect IC, Eldo™. |
| Analog IC layout | Cadence™ Virtuoso Layout/Layout XL flow, Assura, Mentor Graphics™ Calibre. |
| Mixed Signal IC | Cadence™ ICMS/ICFB, AMS-Designer plug-in. |
| Digital IC design | Basic VHDL language and synthesis. |
| PCB design | Basic knowledge of Altium suite. |

## Job skills

| Category | Applications |
|---|---|
| Analog/Mixed signal IC design | Very good knowledge of design methodology for low power/voltage and high voltage analog cells. |
| Analog/Mixed signal IC layout | Very good analog layout experience with parasitic and area optimization. |
| Lab testing | Good knowledge of standard lab instrumentation and experience in samples testing and characterization. |
| Relational skills and flexibility | Availability to travel abroad (short periods); Good relational skills, able to work in dynamic environment with flexible timetable. |

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